AMENDMENTS TO THE SPECIFICATION

IN THE SPECIFICATION:

Page 17, first full paragraph, please amend as follows:

The serial net frame data signal 610 is converted to parallel signals 616 using the 16-bit deserializer 602, or serial-in-parallel-out (SIPO) converter. The deserializer 602 receives net frame data 610 from a corresponding backplane channel along with the 77.76 MHz clock signal 612 and the receive clock enable signal 614. The deserializer 602 converts each 16-bit net frame data unit into 16 parallel signals 616 with each signal representing a corresponding bit of the net frame data unit. These parallel signals 616 are provided to the holding register 604 along with a write clock enable signal (wr_clk_en) 618 and the 77.76 MHz clock signal ~~614~~ 624. Further, the parallel signals (TSNet_unit_n_new) 620 are provided to the receive data memory 606 and the interrupt generator and status circuitry 608.

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Page 34, first full paragraph, please amend as follows:

Figure 29 is a flow diagram for servicing massive interrupts in random access memory (RAM) of an embodiment. In response to receipt of a massive interrupt signal 2902, at least one unit interrupt register is read in a first RAM area 2904. A set unit interrupt bit corresponds to an address in a second RAM area. An interrupt status register is read at the corresponding address in the

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second RAM area in response to the set unit interrupt bit 2906. A set interrupt status bit corresponds to an address in a third RAM area. The interrupt cause bits are read at the corresponding address in the third RAM area in response to the set interrupt status bit 2908, and detailed information is obtained about the interrupt. The interrupt is serviced 2910 in accordance with the detailed information.

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